Blue Pearl Solutions™
ASIC, FPGA, and IP Verification

Analyze RTL AI

Overview

Capture. Analysis. Fix. Validate. From concept to bitstream, Blue Pearl Solutions' Visual Verification Suite provides the tools you need to accelerate verification and improve RTL quality enabling first pass success.

Analyze RTL™ AI provides advanced stimulus free static and formal RTL linting combined with a powerful debug environment to quickly identify critical design issues, up front, streamlining simulation and synthesis while improving overall quality of results. Whether starting with generative AI RTL or a legacy RTL, Analize RTL AI doesn't just find issues, it helps you fix them fast with the power of AI.

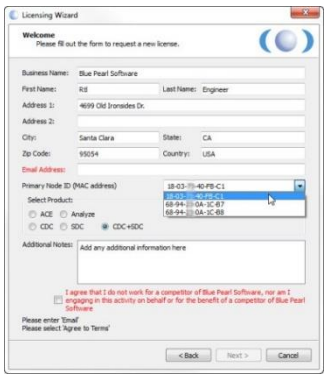
Key Benefits

Modern FPGAs routinely have millions of gates with memories, transceivers, third party IP and processor cores. RTL issues can be time consuming and complex to debug in the lab and through simulations. To reduce verification and debug times, designers need tools that can identify problems quickly before simulation and synthesis, and definitely before spending time in the lab.

Key Features

Analyze RTL accelerates RTL verification and debug:

- Fast and meaningful results with tool Setup Wizard

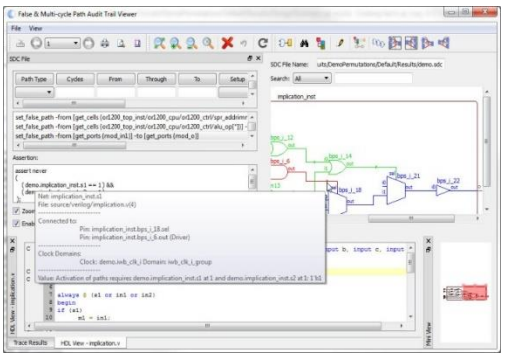


- Checks IEEE Verilog/System Verilog & VHDL language specification compliance and syntax
- Easly configure company specific checks along with standard checks, STARC, DO-254, and Xilinx® UltraFast™ Design Methodology
- Over 400 individual checks
- The GUI to streamlines debug with schematics, FSM diagrams and message viewer and more
- Use message sorting, filtering and waiving to pinpoint problems and track issues that must be fixed and those that are exceptions
- Automated flow with Tcl-based Command Line Interface

Find Design Issues Quickly

The Visual Verification Suite's Analyze RTL enables users to debug design issues quickly using intelligent sorting and message filtering.

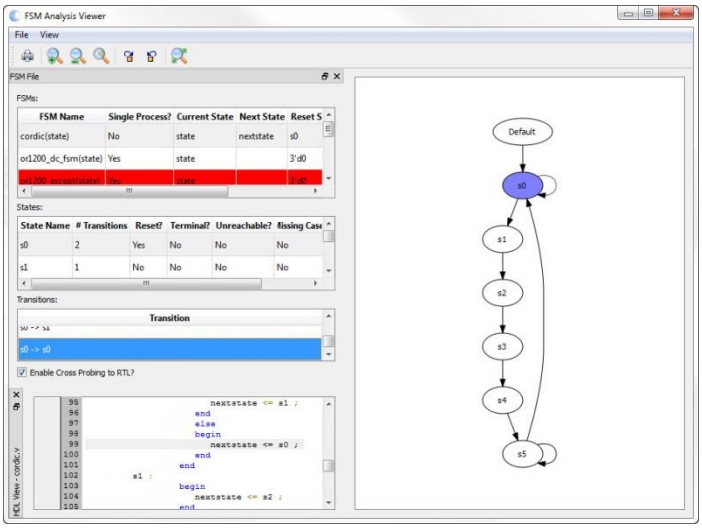
- Low Noise
- Check customization for specific design style
- Easy setup
- Waiver migration



Finite State Machine Analysis

Rather than writing exhaustive simulation test benches to validate their finite state machines (FSMs), designers can use the FSM analysis capability within Analyze RTL. With minimal effort, designers can

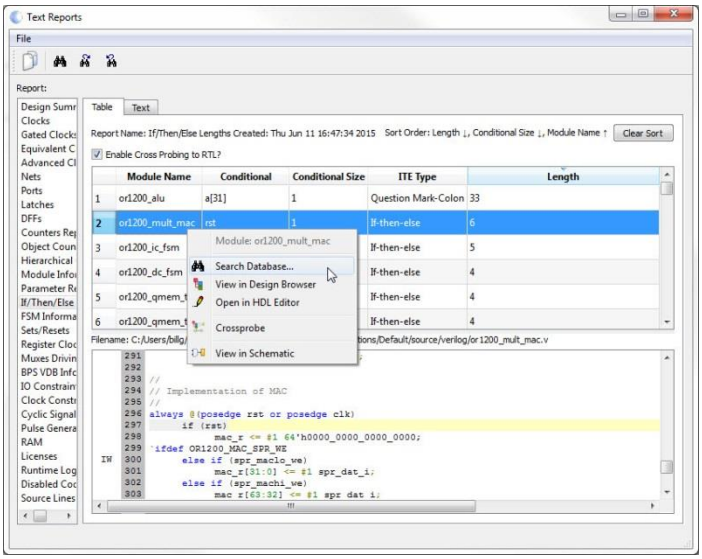
- Extract FSMs from their RTL
- Find dead or unreachable states
- Generate easy to read bubble diagrams to better visualize FSMs



RTL Checks for High-Speed Designs

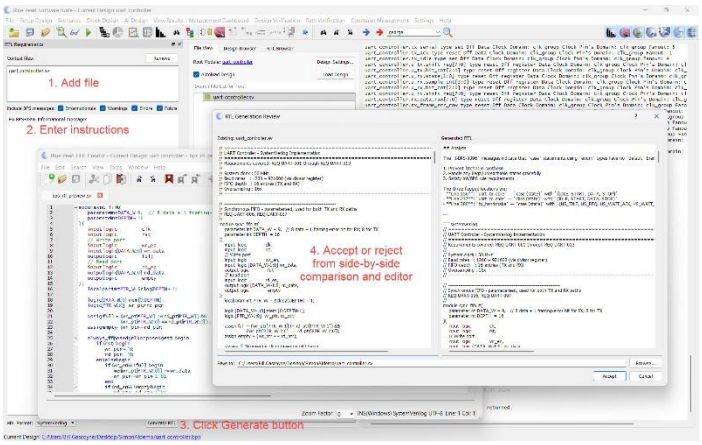
It is important to find as early as possible RTL coding that prevents the design from getting desired speed. In FPGAs, because of their more constrained fabric than ASIC, certain types of structures cause slowdowns. Rather than wait for synthesis or static timing analysis results, Analyze RTL users can easily identify:

- High fanout nets
- Deeply nested “if-then-else” statements
- Long logic paths
- Reset methodology, Async/sync



Fix Issues Fast with AI

Once an issue is found, simply select the code in question, ask your LLM of choice to address the issue, compare and accept the results. With the Integrated AI interface, it’s that easy.



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