Blue Pearl Solutions™
ASIC, FPGA, and IP Verification

CDC and RDC Analysis AI

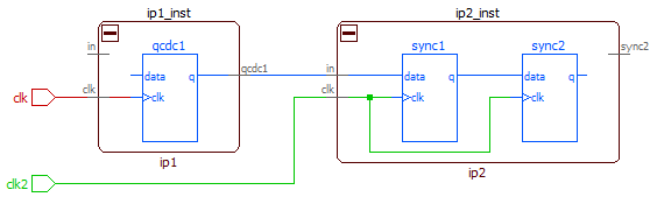
Overview

Capture. Analysis. Fix. Validate. From concept to bitstream, Blue Pearl Solutions' Visual Verification Suite provides the tools you need to accelerate verification and improve RTL quality enabling first pass success.

The Visual Verification Suite offers the capability to analyze, debug and fix with AI, designs with Clock Domain Crossing (CDC) and Reset Domain Crossing (RDC) issues.

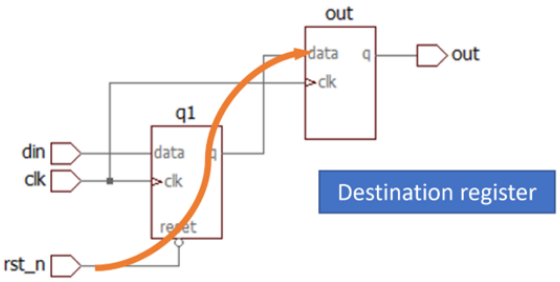
Why CDC Analysis

Today's designs routinely have millions of gates with memories, transceivers, third party IP and processor cores. They have a growing number of clocks that are asynchronous to one another. For data to transfer properly from one asynchronous clock domain to another, there needs to be a synchronizer to capture the data reliably and avoid metastability.

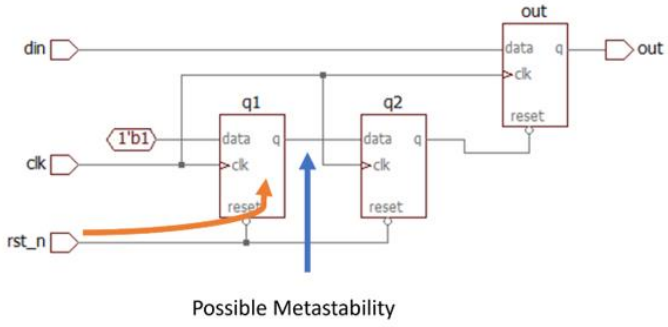


Why RDC Analysis

Reset Domain Crossing (RDC) issues are typical for designs with complex reset strategies that require more frequent reset sequences within certain regions of the design. Proper design analysis of asynchronous reset implementation requires separate analysis of assertion and de-assertion conditions. The reset assertion condition can cause metastability due to a setup/hold time violation on the destination register driven by the register whose reset is asserted. The reset de-assertion condition can cause metastability due to a recovery time violation on the source register when reset is de-asserted.



Reset Assertion

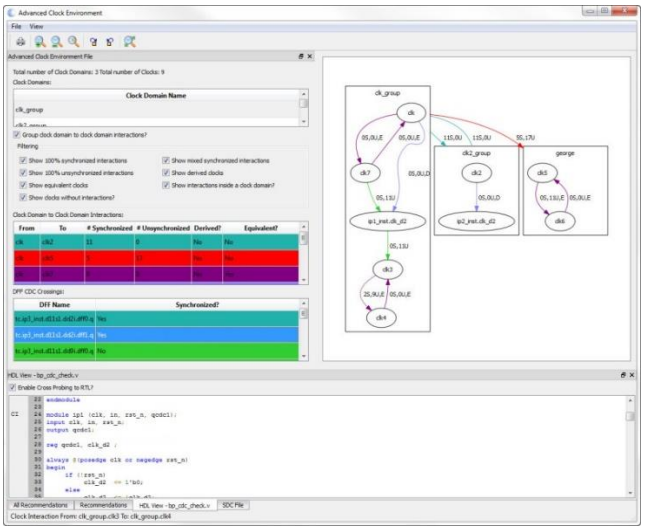


Reset De-assertion

Ease of Setup for CDC Analysis

The suite's Advanced Clock Environment (ACE) solves the iterative and reactive CDC setup problem experienced by designers. It is used before running a CDC analysis. With ACE, designers can clearly see if clocks are not in the intended domains and make corrections before in-depth CDC analysis.

- Automatic Clock and reset identification
- SDC input of domain information
- Understands FPGA clock generator blocks to propagate clocks
- Advanced clock analysis diagram

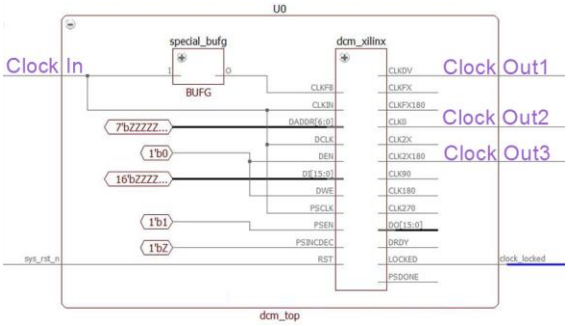


Understands FPGA clock schemes

Most CDC tools do not understand FPGA vendor clocking schemes. Designers thus spend enormous resources to set up their designs. The suite's CDC analysis has built-in intelligence such that with minimal effort, designers can:

- Set up their CDC run
- Debug using the built-in cross-probing and schematic display.

Generated clocks from FPGA IP clock distribution module are in the same domain. This eases setup and minimizes false CDCs.



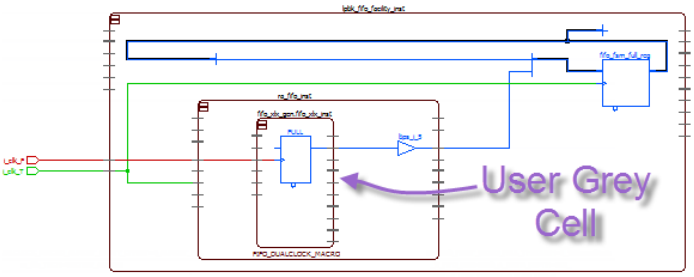
RDC Analysis Types

The Suite's RDC verification solution identifies asynchronous reset assertion and de-assertion that can cause critical metastability issues at reset domain crossings, and glitches due to combinational resets. In addition, there are also approximately two dozen available checks that look at other aspects of reset implementation apart from assertion or de-assertion analysis.

Hierarchical CDC/RDC analysis for IP-based designs

In a typical flow, designers need to black box their generated or non-synthesizable IP. The resulting CDC analysis is incomplete and does not report many CDC issues that lead to metastability in the field. With Blue Pearl's User Grey Cell™ (UGC) methodology, CDC and RDC issues across boundary interfaces can be identified before they become an issue.

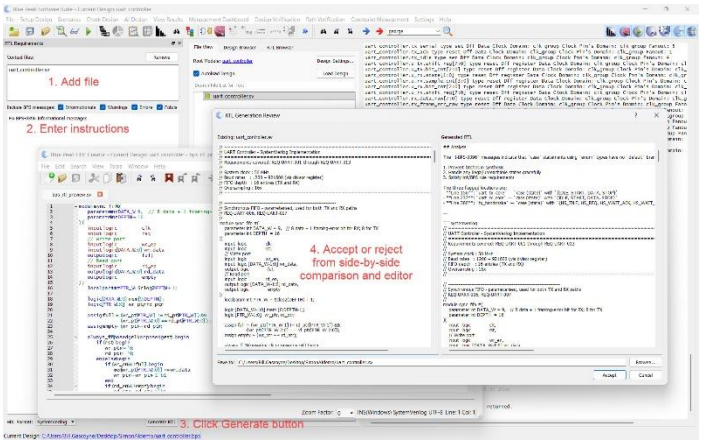
- The Visual Verification Suite release contains FPGA vendor UGC models
- UGC are easy to create from a data book
- Automated User Grey Cell editor streamlines development



User Grey Cell

Fix Issues Fast with AI

Once an issue is found, simply select the code in question, ask your LLM of choice to address the issue, compare and accept the results. With the Integrated AI interface, it's that easy.



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